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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,133	10/23/2003	Charles A. Miller	FACT-01000US0	1801

23910 7590 03/07/2005

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EXAMINER	
KOBERT, RUSSELL MARC	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 03/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,133	MILLER, CHARLES A.	
	Examiner	Art Unit	
	Russell M. Kobert	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14,15 and 19-23* is/are rejected.

7)☒ Claim(s) *2-13 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 14, 15 and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Miller (6622103).

Miller anticipates (Figures 3 and 4) an apparatus comprising: a variable delay isolation buffer (40) having a signal input (DRIVE), a variable delay control input (Z), and an output (portion connected to node 34); and a delay control circuit (46) having an output (Z) providing the variable delay control input of the variable delay isolation buffer, the delay control circuit setting a delay control voltage potential at its output to control delay through the variable delay isolation buffer to substantially match delay through a time delay reference (column 6, line 30 - column 7, line 67); as recited in claim 1.

Miller anticipates (Figures 3 and 4) a test system comprising: a tester (10) for transmitting and receiving test signals for testing devices on a wafer (column 5, lines 30-33, 36-39); isolation buffers (40) having inputs connected in common to a tester (series of TESTER CHANNELs 26), each one of the isolation buffers further having an output (portion connected to node 34); and probes (24) each configured (see Figure 1) to

contact one of the devices on the wafer (14), and each of the probes further having a terminal (portion of 24 connected to pogo pins 22 and further connected to isolation buffer 40 via nodes 34) connected to the output of one of the isolation buffers; as recited in claim 14.

As to claim 15, having a variable delay control input (Z) for receiving a variable voltage potential set to control a time delay of a signal between the input (DRIVE) and output (portion connected to node 34) of the respective isolation buffer, the test system further comprising: a delay control circuit (46) having an output (Z) connected to the variable delay control input of the isolation buffers, the delay control circuit setting a magnitude of a control voltage potential at its output based on a time delay reference (column 6, line 30 - column 7, line 67) is anticipated by Miller.

Miller anticipates a method of testing integrated circuits (12) on a wafer (14) comprising: supplying test data signals from a tester to be distributed from a tester channel (26) to one of a plurality of probes (24) configured to connect to test pads on an integrated circuit (1C); and distributing the channel through isolation buffers (40) to multiple branches (pins 22 within probe card 20), each branch being connected to one of the plurality of probes; as recited in claim 19.

As to claim 20, controlling delay through the isolation buffers so that each isolation buffer provides substantially the same delay is considered inherent to Miller because the objective in Miller is to calibrate the timing of the tester channels (column 1, lines 7-12; column 2, lines 19-45).

As to claim 21, having the step of controlling delay through the isolation buffers

controls delay by varying a power supply voltage applied to the isolation buffers is considered inherent because Miller's operation as disclosed controls signal Z when driving tri-state buffer 40.

As to claim 22, having the step of controlling delay through the isolation buffers controls delay by varying current through the isolation buffers is considered inherent because Miller's operation as disclosed controls signal Z when driving tri-state buffer 40.

As to claim 23, providing a variable delay buffer (40) in the channel (26) prior to the multiple branches (pins 22 within probe card 20); and controlling delay of the variable delay buffer to provide substantially the same delay through the each of the multiple branches (column 6, line 30 - column 7, line 67) is anticipated by Miller.

3. Claims 19, 20 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon et al (5070297).

Kwon et al anticipates (Figure 3) a method of testing integrated circuits (42, 44, ...) on a wafer (that which full wafer probe card 10 is configured to engage) comprising: supplying test data signals from a tester (40) to be distributed from a tester channel (78, 80, 82, 84, 86, 88, 90) to one of a plurality of probes (16) configured to connect to test pads (19) on an integrated circuit (IC CHIPs 42, 44, ...); and distributing the channel through isolation buffers (46, 48) to multiple branches (that portion of 16 connected to buffers 46 and 48), each branch being connected to one of the plurality of probes; as recited in claim 19.

As to claim 20, controlling delay through the isolation buffers so that each

isolation buffer provides substantially the same delay is considered inherent to Kwon et al (column 5, lines 56-59).

As to claim 23, providing a variable delay buffer (46, 48) in the channel prior to the multiple branches; and controlling delay of the variable delay buffer to provide substantially the same delay through the each of the multiple branches (column 5, lines 56-59) is anticipated by Kwon et al.

4. The following is a statement of reasons for the indication of allowable subject matter:

Claims 2-13 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The additional limitation of a reference delay line; a reference buffer having a signal input, a variable delay control input, and an output; and a phase comparator having a first input connected to reference delay line, a second input connected to the output of the reference buffer, and having an output connected to the variable delay control inputs of the reference buffer and the variable delay isolation buffer as further described in claim 2 has not been found.

The additional limitation of driver buffers each having a signal input connected to the output of the variable delay isolation buffer, and a power supply input connected to receive a system voltage as further described in claim 4 has not been found.

The additional limitation of the variable delay isolation buffer comprises a

differential amplifier with a variable current sink providing the variable delay control input as further described in claim 6 has not been found.

The additional limitation of the variable delay isolation buffer comprises a first variable delay isolation buffer, the apparatus further comprising: additional variable delay isolation buffers each having a signal input connected in common with the first variable delay isolation buffer, a variable delay control input connected to the output of the delay control circuit, and having an output as further described in claim 12 has not been found.

The additional limitation of driver buffers each connecting the output of one of the isolation buffers to one of the probes, and each having a power supply input connected to receive the system voltage as further described in claim 16 has not been found.

The additional limitation of an oscillator, a reference delay line providing the time delay reference, the reference delay line having an input connected to the oscillator, and having an output; a reference buffer having a signal input connected to the oscillator, a variable delay control input, and having an output; and a phase comparator having a first input connected to the output of the reference delay line and a second input connected to the output of the reference buffer, and having an output connected to the variable delay control inputs of the reference buffer and the isolation buffers as further described in claim 17 has not been found.

The additional limitation of each of the isolation buffers has a power supply input connected to receive the system power supply voltage, the test system further comprising: a variable delay control buffer connecting the inputs of the isolation buffers

to the tester, the variable delay control buffer further having a variable delay control input; and a delay control circuit having an output connected to the variable delay control input of the variable delay control buffer, the delay control circuit setting a delay control voltage potential at its output based on a time delay reference as further described in claim 18 has not been found.

It is further noted that the examiner's reasons are understood to be predicated upon consideration of each of the claims as a whole, and not upon any specific elements of the claims.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mayder et al (6570397) shows a method applying timing error offsets to test channels in a test head.

Tomita et al (6181145) shows a test chip having a tri-state buffer used to facilitate the test of a time delay (col 5, ln 34-42).

6. A shortened statutory period for response to this action is set to expire three month(s) from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russell Kobert whose telephone number is (571) 272-1963. The Examiner's Supervisor, Nestor R. Ramirez, can be reached at (571) 272-2034. For an automated menu of Tech Center 2800 phone numbers call (571) 272-2800.

Russell M. Kobert
Patent Examiner
Group Art Unit 2829
March 2, 2005

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PRIMARY EXAMINER
A.U. 2829
03/03/05